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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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[REDACTED] EXAMINER

RUGGLES, JOHN S

ART UNIT	PAPER NUMBER
	1756

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,428	PIERRAT ET AL.	
	Examiner	Art Unit	
	John Ruggles	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 04 February 2003 and 01 August 2002.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-55 is/are pending in the application.
- 4a) Of the above claim(s) 1-22 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 23-31,33-34,36-55 is/are rejected.
- 7) Claim(s) 23-55 is/are objected to.
- 8) Claim(s) 1-55 are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 05 October 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>4,5,6</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-14, 20, drawn to a method of analyzing and responsive configuring for optical lithography to fabricate an integrated circuit, classified in class 430, subclass 30.
- II. Claims 15-19, 21-22, drawn to a reticle for use in optical lithography, classified in class 430, subclass 5.
- III. Claims 23-55, drawn to a method of manufacturing an integrated circuit by patterned optical lithographic exposure, classified in class 430, subclass 311.

Inventions II and I, III are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In this case, the reticle product can be used in a materially different process, such as single exposure through the reticle of a photoresist layer to manufacture a non-electrical product, without involving analyzing, configuring, or setting parameters as recited in the processes of Groups I and III.

Inventions I and III are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different

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inventions are not useable together and have different modes of operation. Groups I and III are distinct inventions because Group I recites a process of analyzing pattern layout data and configuring an optical lithography system with optical parameters in response to prior analysis while Group III recites a process of manufacturing an integrated circuit by actual exposure of a photosensitive resist through mask (reticle) patterns, without analyzing a pattern and responsive configuring for the exposure.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mark Haynes on 22 April 2003, a provisional election was made without traverse to prosecute the invention of Group III, claims 23-55. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-22 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to non-elected inventions.

Specification

The disclosure is objected to because of the following informalities: (1) “settings that do the features” should be corrected to --settings than do the features-- in line 20 on page 8; (2) “of a in a functional unit of’ should be changed to --of functional units in-- in line 19 on page 9; (3) “substantially of” should be corrected to --substantially all of-- in line 3 on page 10; (4) “both a phase shifting and trim patterns” should be corrected to --both phase shifting and trim patterns-- in line 15 on page 11; (5) “trim and binary” should be changed to --phase shifting and trim-- in

line 25 on page 11, if this best represents applicant's intention in the original specification; (6) "ration" should be corrected to --ratio-- in line 11, "provides method" should be --provides a method-- in line 19, and "Method" should be --The method-- in line 20, all on page 12; (7) "form of features an integrated circuit" should be changed to --form integrated circuit features-- in line 11, "on integrated circuit" should be --on an integrated circuit-- in line 13, and "controlled the effect of exposure" should be just --controlled--, all on page 13; and (8) "refers processes" should be corrected to --refers to processes-- in line 12 on page 14.

Appropriate correction is required.

Claim Objections

Claims 23-55 are objected to because of the following informalities: (1) in claim 23, "An method" should be changed to --A method-- in line 1 and "exposing layer of material" should be corrected to --exposing the layer of material-- in line 7, to be grammatically correct; (2) in line 2 of claims 25, 46 and 54, "ninety-five" should be corrected to --ninety-five percent--; (3) in line 1 of claim 30, "of manufacturing an IC product of manufacturing an IC product" is repetitive and must be corrected to --of manufacturing an IC product--; (4) in line 3 of claim 31, "dosing in" should be reworded as --dosing being in--, to be grammatically correct; (5) in line 4 of claim 36, "by set" should be corrected to --by a set--, to be grammatically correct; (6) in line 8 of claim 48, "setting of set" should be corrected to --setting of the set--, to be grammatically correct. Claims 24-35 are dependent on claim 23, claims 37-47 are dependent on claim 36, and claims 49-55 are dependent on claim 48. Appropriate correction is required.

Claim 24 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. See MPEP § 608.01(n). Claim 24 is also objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim (non-existent claim 0). Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Accordingly, claim 24 has not been further treated on the merits.

Applicant is advised that should claim 27 be found allowable, claim 33 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. Since claims 34-35 are dependent on claim 33, they would also be objected to on this basis. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 24, 45, and 53 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The phrase "eighty percent (80%) of non-memory portions" in regard to mask pattern

layout found in lines 4-5 of claim 24 and lines 2-3 of claims 45 and 53 is not enabled by the specification. While this phrase is found in the specification at line 12 on page 9, no explanation is given to enable one of ordinary skill in the art to clearly understand the intended meaning of “non-memory” in regard to the mask pattern. In this instance, mere statement of this phrase in the specification does not enable the claims, because the meaning of this phrase has not been defined and is open to misinterpretation. Since many integrated circuit products made by photolithography are memory devices (e.g., transistor gates for a DRAM, etc.), it is likely that applicant intends to use the phase shift pattern mask to define at least eighty percent (80%) of the (pattern) portions that do not form memory devices. Accordingly, for the purpose of this Office action and in order to advance prosecution of this application, the examiner has interpreted this phrase to mean --eighty percent (80%) of the pattern portions not defining memory devices--. However, claims 24, 45, and 53 must still be amended in response to this rejection.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23-35, 38, 45, and 53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 23, it is unclear whether “the pattern” being protected in line 5 is the pattern made in the layer of material, the first pattern made by the first (phase shifting) mask, the second pattern made by the second (trim) mask, or some other recited pattern such as either the first (phase shifting) or the second (trim) mask pattern. For the purpose of this Office action, the

examiner has interpreted “the pattern” being protected in line 5 to mean --the first pattern made in the layer of material by the phase shifting mask (first mask)--. Furthermore, it is not clear what is meant by “defining” in line 2, since the patterns would not be defined in the layer of material apart from actual exposure, recited as a separate step of “exposing layer of material” in line 7. Therefore, the examiner has interpreted the “defining” of line 2 and the “exposing” of line 7 to be descriptions of the same exposure step. However, claim 23 must still be amended in response to this rejection. Claims 24-35 are dependent on claim 23.

Claim 24 must be in one sentence form only. Note the format of the claims in the patent(s) cited. In line 6, “the floorplan” lacks antecedent basis. Also, claim 24 is rendered indefinite by dependence on non-existent claim 0, found at line 3. Furthermore, the phrase “at least eighty percent (80%) of a part of the floorplan” (emphasis added) in reference to the portion defined by the phase shift pattern (lines 5-6) is indefinite so as to prevent determination of the metes and bounds of this claim (i.e., a part ranges from 0-100% of the whole (floorplan) so at least 80% of 0-100% is still 0-100% and it is unclear how this statement further limits the scope of this claim). Accordingly, claim 24 has not been further treated on the merits.

In claims 28-29 and 38, the phrase “the numerical aperture” found in line 2 lacks antecedent basis.

In claims 45 and 53 at lines 4-5, “the floorplan” and “the critical path” both lack antecedent basis. Also, in claims 45 and 53, the phrase “at least eighty percent (80%) of a part of the floorplan” (emphasis added) in reference to the portion defined by the phase shift pattern (found at lines 3-4 of both claims) is indefinite so as to prevent determination of the metes and bounds of these claims (i.e., a part ranges from 0-100% of the whole (floorplan) so at least 80%

of 0-100% is still 0-100% and it is unclear how this statement further limits the scope of these claims). Accordingly, for the purpose of this Office action, the examiner has interpreted these claims without this limitation (i.e., as if it were not there), since it does not clearly limit the scope of either of these claims. However, claims 45 and 53 must still be amended in response to this rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 36-38 and 48-52 are rejected under 35 U.S.C. 102(b) as being anticipated by Spence (US Patent 5,573,890).

Spence teaches a photolithography (an optical lithography) process of manufacturing an integrated circuit (IC) having a gate pattern using a phase shift mask (PSM) pattern to expose a resist layer on a wafer (understood to encompass forming a resist layer on a wafer in a first process station (e.g., for coating resist on wafer, etc.) and subsequently moving the resist coated wafer to a second process station (optical lithography system stepper shown in Figure 2(e)) for patterned exposure of the resist). The PSM is designed to reliably shrink gate size for logic circuits (column 4, lines 37-38). The process of manufacturing the circuit involves exposing (defining and exposing in a single step) a resist layer through the patterned PSM shown in Figure

6 to make the circuit shown in Figure 3 (column 5, lines 40-44). Alternatively, a two step exposure process involving first exposure (by a first dose of radiation using a first setting of optical parameters) of the resist through the patterned PSM of Figure 7 followed by second exposure (by a second dose of radiation using a second setting of optical parameters which may or may not be the same as the first dose and/or may or may not utilize the same setting of optical parameters as the first dose) through the patterned trim mask of Figure 8 to remove unwanted dark lines (clearing phase shifting artifacts) described at column 5, lines 45-59 (instant claim 36). The gate shrink feature shown in Figure 11(b) was manufactured with a wafer stepper exposure apparatus (optical lithography system) such as that shown in Figure 2(e) using either (1) the natural dark line formed by abutting 0° and 180° phase shift regions on the PSM (column 6, lines 30-32) or (2) a narrow opaque line 75 on the mask to overlay the natural dark abutting transition between 0° and 180° phase shift regions on the PSM (column 6, lines 36-42). In order to make this gate shrink feature, column 6, lines 33-36 specify setting the following optical parameters of the optical lithography system: numerical aperture, wavelength of exposure radiation, and light source partial coherence (instant claim 37 for partial coherence (σ); instant claim 38 for numerical aperture (NA); instant claim 48 for numerical aperture, wavelength of radiation, and/or (partial) coherence; instant claim 49 for numerical aperture and partial coherence; instant claim 50 for numerical aperture and/or partial coherence; instant claim 51 for partial coherence as the coherence parameter; and instant claim 52 for different dosage levels).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 23, 25-26, 28-30, 40-41, 45-46, and 53-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spence as applied to claims 36-38 and 48-52 above in view of Jinbo, et al. (“0.2 μm or Less Lithography by Phase-Shifting-Mask Technology”, 1990, IEEE, pages 33.3.1-33.3.4).

Spence does not teach that the PSM defines substantially the entire integrated circuit (IC) pattern or that the setting of optical parameters is substantially the same while exposing the resist by the PSM and trim mask patterns. Spence also does not teach setting optical parameters including illumination configuration and/or defocus of the exposure radiation.

Jinbo describes a lithography process using PSMs (having phase-shifter edge lines (PEL)) “which basically consist of only shifter patterns” (taken to be referring to “full phase shift” or “full phase” masks defining substantially all of a circuit pattern, found in the 4th paragraph (¶) of the Introduction section at the 2nd column on page 33.3.1; reads on: instant claim 25 for at least 95% of the overall pattern defined by a PSM; instant claims 45 and 53 for at least 90% of the overall pattern defined by a PSM, all features in the critical path (features having a critical dimension (CD)) defined by a PSM, and/or all features that are not phase shifted due to phase conflicts defined by a PSM; and instant claims 46 and 54 for a pattern characterized

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by having at least 95% of the overall pattern defined by a PSM). The resulting light intensity pattern formed by the PEL is found to be “shaper” (understood to mean --sharper--) than that obtained from a chrome mask (binary mask, non-PSM) in a stepper optical exposure system (instant claim 26 for a stepper) when compared under the same illumination conditions (illumination configuration, instant claim 40) or substantially the same illumination conditions (substantially the same setting of optical parameters that control characteristics of exposure, instant claim 23). Substantially the same setting of optical parameters reads on “within plus or minus 10%”, instant claim 30). The following illumination conditions (optical parameter settings) were substantially the same to allow comparison: numerical aperture, exposure wavelength, coherence factor (partial coherence), and/or defocus position (defocus, page 33.3.1, in the 2nd column, under the Concept of a Phase-shifter Edge Line Mask section; instant claims 28-29 and 40-41). The use of PSM lithography is expected to meet the drive toward denser and higher-speed devices (e.g., DRAM, etc.) by improving resolution of substantially all photolithographic patterns (which includes memory and/or non-memory devices; reads on instant claims 45 and 53 for at least 80% of the non-memory (device) portions of the overall pattern defined by a PSM) as explained in the Introduction and Conclusion sections, found in the 1st column on page 33.3.1 and in the 2nd column on page 33.3.2, respectively.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) taught by Spence for shrinking a transistor gate in an IC with the full PSM lithography process to define substantially all of the circuit pattern (including memory and/or non-memory devices) using substantially the same exposure illumination optical parameter

settings for PSM and trim (binary) mask exposures as described by Jinbo. This is because the PSM pattern features are sharper (have better resolution) than those obtainable with only a binary mask as explained by Jinbo to meet the drive toward denser and higher-speed devices (e.g., DRAM, non-memory devices, etc., by allowing definition of smaller feature size patterns).

Claims 25, 45-46, and 53-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spence and Jinbo as applied above, and further in view of Wong, et al. ("Investigating Phase-Shifting Mask Layout Issues Using a CAD Toolkit", 1991, IEEE, pages 27.4.1-27.4.4).

While teaching at least some portion of all the limitations found in claims 25, 45-46, and 53-54 as pointed out above for a PSM and trim mask photolithography process (by single or plural separate exposures to pattern a resist layer on a wafer) in which the PSM is a full PSM defining substantially the entire overall pattern, Spence and Jinbo do not specify a lower percentage of the overall pattern defined by the PSM or address how to resolve phase conflicts when they arise (possibly preventing 100% of the overall pattern from being defined by a PSM).

Wong shows CAD layout of a PSM for a photolithography process to pattern a mask layer (e.g., resist on a wafer, etc.) for manufacturing a DRAM having a non-regular cell pattern in which at least 94% of the patterned cell area is easily shiftable (defined) using two phases (for the PSM, to shrink pattern dimensions by defining at least 94% of the overall pattern by a PSM) and recommends solutions for remaining difficult areas (to define a larger percentage of the overall pattern by imaging through a PSM, according to the abstract in the 1st column on page 27.4.1). Also in the first column on page 27.4.1, the 2nd ¶ of the introduction describes the shaded areas of Figure 1 to be phase conflict areas (remaining difficult areas) in which closely

spaced geometries have the same phase, making up about 1% of the total cell area and about 6% of the edges. The conflict areas are reduced by CAD analysis and redesign to eliminate some of the phase conflicts (allowing these conflict areas of the overall pattern to still be reduced in size (shrunk) by use of a PSM) or at least partially convert the conflict areas to conflict-free areas (e.g., by using additional phases in these areas of the PSM, etc.). These methods reduce the violation (difficult or phase conflict) area and further increase chip shrinkage (to increase the proportion of the overall pattern defined by a PSM to greater than 94%) as described in the last ¶ of the DRAM Investigation Results section found in the 1st column on page 27.4.2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) taught by Spence for shrinking a circuit with at least 94% of the overall pattern defined by the PSM designed by CAD as shown by Wong (encompasses instant claims 25, 46, and 54 for at least 95% of the overall pattern defined by a PSM; reads on instant claims 45 and 53 for at least 80% of the non-memory portions of the overall pattern defined by a PSM, at least 90% of the overall pattern defined by a PSM, and all the features in the overall pattern defined by a PSM except those not phase shifted due to phase conflicts; and renders obvious instant claims 45 and 53 for all the features in the critical path (critical dimensions, CD) of the overall pattern defined by a PSM, and/or everything in the overall pattern except test and/or dummy structures (not critical) defined by a PSM). This is because the PSM pattern features increase chip shrinkage by decreasing pattern dimensions. Therefore, the highest percentage of the overall pattern that can be defined by PSM features (e.g., by reducing phase conflicts in

difficult areas, etc.) during photolithography will be expected to result in the greatest dimension reduction.

Claims 27 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spence and either Jinbo or Wong as applied above, and further in view of Pierrat (US Patent 6,040,892).

While teaching a PSM and trim mask photolithography process (by single or plural separate exposures to pattern a resist layer on a wafer) in which the PSM is either a full PSM defining substantially the entire overall pattern (Jinbo) or a PSM defining at least 94% of the overall pattern (Wong), Spence and either Jinbo or Wong do not specify that the PSM and trim masks are on the same reticle and do not describe blading the PSM and trim masks during exposure to permit different dosing through these masks.

Pierrat discloses optical lithographic techniques (photolithographic processes) for patterned exposure (including multiple exposures to different patterns) of a resist layer on a semiconductor wafer and a corresponding reticle having multiple mask patterns (including PSMs) on the same reticle shown in Figure 1 to form a circuit pattern (column 1, lines 10-15, column 3, lines 39-51, and column 4, lines 4-20; instant claims 27 and 33). As shown in Figure 2 and described at column 4, lines 35-57, the different masks on the reticle 211 are selectively exposed (differently dosed) to project these patterns onto the semiconductor wafer (to image a resist layer on the wafer). The different dosing of the masks is controlled by selective mechanical movement of aperture blades 216, 218, 220, and 222 (blading, instant claim 34) to open a selective area aperture 214 and allow light from the source 212 that has been imaged by at

least one of the masks to expose a patterned image area onto the resist. The wafer is moved and aligned with respect to the masks on the reticle by a conventional stepper 230 (optical lithography system). Multiple exposures through different masks (including a PSM) allow undesired imaged lines (phase shifting artifacts) in the pattern to be removed (phase shift artifacts are cleared) by a second complementary (trim) mask exposure overlapping these undesired lines before further processing (developing) of the resist image (column 5, line 54 to column 6, line 12). Placing the masks on a single reticle simplifies alignment and saves cost when manufacturing complex circuits and devices (column 5, lines 1-4 and 24-28). Moving and/or sizing the aperture by blading controls which image is projected and where it is projected (column 5, lines 5-7 and 29-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) taught by Spence and either Jinbo or Wong with use of the PSM and trim mask on a single reticle which are differently dosed by blading as disclosed by Pierrat. This is because placing the masks on a single reticle simplifies alignment in the stepper and blading allows moving and sizing of the projection aperture (it would also have been obvious to change the exposure intensity or dosage by controlling the time period over which the aperture is open for each mask pattern (understood to be a well known function for a camera aperture) to prevent imaging of unwanted phase shifting artifacts).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spence and Jinbo as discussed above, and further in view of either Pierrat or Borodovsky (US Patent 5,424,154).

While teaching a PSM and trim mask photolithography process (by single or plural separate exposures), Spence and Jinbo do not teach a specific dosing ratio (or point out reasons for using a different dosing ratio) for the PSM and trim mask exposures which satisfies the ratio of 1.0 to r where $r > 0$.

The teachings of Spence and Pierrat are discussed above.

Borodovsky teaches a lithographic process for making a semiconductor device (e.g., logic circuit transistor gate structure, etc.) with enhanced resolution by either exposure of a resist layer through a PSM (and then a complementary (trim) mask) or using oblique illumination (off-axis exposure at an oblique angle to the resist rather than the 90° angle conventionally used – this suggests a purpose for setting the exposure radiation axis of propagation at the resist layer and the illumination configuration (depending on the light source) during exposure) to expose a mask pattern on a resist layer (column 1, line 47 to column 2, line 7). In the PSM alternative, the first PSM exposure is followed by a complementary (trim) mask exposure (column 4, line 3 to column 5, line 61). The resolution of the imaged pattern is shown to depend on optical lens numerical aperture and wavelength of exposure radiation at column 1, lines 20-31. Periodic structures are reproduced with increased resolution and typically have less variation in linewidth due to varying defocus (column 2, lines 36-38). These statements suggest reasons for setting optical parameters during exposure to include the following: lens numerical aperture, wavelength, illumination configuration, defocus, and axis of propagation at the resist layer. The importance of using a complementary (trim) reticle (mask) in improving contrast (enhancing resolution) increases as the feature size decreases (column 8, lines 21-23). Borodovsky specifically points out that at smaller dimensions, the exposure doses for both reticles (masks)

must be adjusted (differently) to provide for complete exposure of the spaces without overexposure of the lines for a resulting composite intensity (total exposure dose) having sufficient contrast (column 8, lines 31-40). The exposure dose for each mask depends on the specific lithographic process and features being formed, and some experimentation with exposure parameters for both reticles (masks) may be necessary to achieve acceptable resolution (column 8, lines 35-40). This is taken to mean that the setting of a dosing ratio between first exposure through the PSM and second exposure through the complementary (trim) mask is highly dependent on the overall configuration in the optical lithography system, in order to obtain the best resolution. Therefore, setting of only the dosing ratio without also specifying appropriate limitations for all other relevant optical parameters would not ensure the best resolution.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) as taught by Spence and Jinbo with adjusted (different) dosing for the PSM and trim mask exposures as taught by either Pierrat or Borodovsky. This is in order to either (1) allow appropriate exposure through different sized bladed apertures as disclosed by Pierrat or (2) improve pattern resolution by providing complete exposure of pattern spaces without overexposure of pattern lines for a resulting composite intensity (total exposure dose) having sufficient contrast as pointed out by Borodovsky. This renders obvious at least a portion of the dosing ratio for the PSM and trim mask exposures which satisfies the ratio of 1.0 to r where $r > 0$ as specified in instant claim 31 (e.g., even the same dosing ratio for PSM to trim mask exposures reads on this range and would be expressed as 1:1 or 1.0 to r where $r = 1.0$, etc.).

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spence as discussed above in view of Borodovsky.

The teaching of Spence as discussed above is drawn to a PSM and trim photolithography process including setting numerical aperture and partial coherence, but does not specifically include setting the following exposure radiation parameters: illumination configuration, defocus, and axis of propagation at the resist layer.

The teaching of Borodovsky is discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) involving setting of optical parameters including numerical aperture and partial coherence as taught by Spence with setting of additional optical parameters including illumination configuration, defocus, and axis of propagation of exposure radiation at the resist layer as taught by Borodovsky to obtain better contrast and enhance resolution as explained by Borodovsky.

Claims 43-44, 47, and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spence as discussed above in view of Pierrat (US Patent 6,040,892).

While teaching a PSM and trim mask photolithography process (by single or plural separate exposures to pattern a resist layer on a wafer), Spence does not specify that the PSM and trim masks are on the same reticle and does not describe blading the PSM and trim masks during

exposure to permit different dosing through these masks. Spence also does not point out that an optical parameter setting is changed by mechanical adjustment of an optical element.

The teachings of Spence and Pierrat are discussed above.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PSM and trim mask photolithography process (by single or plural separate exposures) taught by Spence with use of the PSM and trim mask on a single reticle or mask (instant claim 44) which are differently dosed (instant claim 43) by blading as disclosed by Pierrat. This is because placing the masks on a single reticle simplifies alignment in the stepper and blading allows moving and sizing of the projection aperture (it would also have been obvious to change the exposure intensity or dosage by controlling the time period over which the aperture is open for each mask pattern (understood to be a well known function for a camera aperture) to prevent imaging of unwanted phase shifting artifacts). Furthermore, it would have been obvious to change at least one optical parameter setting in the Spence process by mechanical adjustment of an optical element, because a blading aperture was mechanically moved or sized (affecting the overall optical configuration) as disclosed by Pierrat (instant claims 47 and 55).

Allowable Subject Matter

Claims 32 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: while the concept of different dosing between the PSM exposure and subsequent overlapping trim mask exposure of a resist layer in integrated circuit (IC) manufacture to obtain the smallest features with the best resolution are not new, the specific dosing ratio of 1.0 (for the PSM) to r (for the trim mask) where $2 \leq r \leq 4$ of instant claim 32 and, more specifically, 1:2 (PSM:trim mask) of instant claim 35 are both distinguished over the prior art (which does not teach these specific ratios).

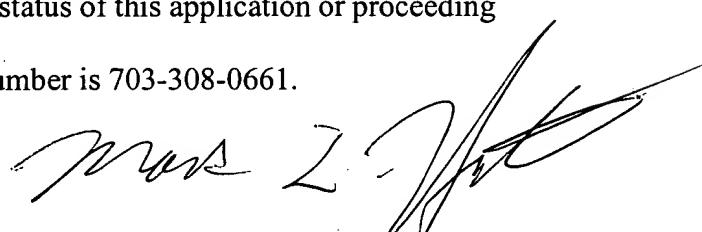
As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Ruggles whose telephone number is 703-305-7035. The examiner can normally be reached on Monday-Thursday and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 703-308-2464. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.



MARK F. HUFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

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Art Unit 1756